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EXAMINER	
BANANKHAH, MAJID A	
ART UNIT	**PAPER NUMBER**
2127	

DATE MAILED: 02/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/458,551	JOFFE ET AL.	
	Examiner	Art Unit	
	Majid A Banankhah	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14,15,17-31,34-51,54-64 and 66-70* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14,15,17-31,34-51,54-64 and 66-70* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This office action is in response to the amendment and remarks filed on November 29 2004. Applicant's arguments have been fully considered but they not deemed to be persuasive Applicant's amendment necessitated the new ground of rejection. Claims 14-15, 17-31, 34-51, 54-64, and 66-70 are considered for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 14-15, 17, 23-24, 30-31, 34-36, 50-51, 54-56, and 69-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okin (U.S.Pat. No. 5,361,337, 'Okin') in view of Hendel et al. (U.S.Pat. No. 5,175,732, 'Hendel').

Per claims 14, and 23, the reference of Okin teaches of:
a processor for executing instructions such that when the processor executes a first instruction accessing a resource and the processor determines after starting to execute the first instruction that the first instruction is blocked due to the resource being unavailable for the first instruction (col. 3, lines 56-61, when a cache miss occurs, and col. 5, claim 6, lines 11-25, suspending execution of the first process when encountering a first cache miss while executing a first process, also note in col. 2, lines 29-36, Having multiple copies of state elements on the processor and coupling them to a multiplexer permits the processor **to save the context of the current instructions** and **resume executing new instructions within one clock cycle**).

The system of Okin does not care whether the resource is cache miss or FIFO. In other words, the functionality of the suspension of the instruction does not change whether the resource is of one kind or another. However, in order to show FIFO as a resource, the Examiner is citing the reference of Hendel to show resource could be a FIFO storage unit as well. The system of Hendel discloses a networking environment wherein the command and status interface unit further comprises **command routing means** for selectively **routing the receive commands to the first FIFO storage unit, the transmit commands to the second FIFO storage unit, miscellaneous commands** to the medium access control unit, and clearing commands to the third and fourth FIFO storage units. Later he teaches of request FIFO, command FIFO, and status FIFO in col. 10, lines 55, line 55 to col. 11, line 7. Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to use Okin's modified processor in the networking environment of Hendel, for the reason to minimize the average instruction cycle time for the processor with a main memory access time.
Therefore, it is obvious to use Okin's processor for any environment including network data FIFO storage unit as a resource as evidenced by Hendel, for the reason to minimize the average instruction cycle time for the processor with a main memory access time exceeding processor clock cycle.

Per claim 15, the processor of claim 14 wherein the processor executes the first instruction to completion when the FIFO becomes available. The reference of Okin teaches of the limitation in claim 2 (switching back to execute said previously suspended first process by said stateless elements upon suspending said second process if data fetching from said main memory into said cache memory by said cache and main memory as a result of said first cache miss has been completed).

Per claim 17, the system of Okin teaches multitasking in col. 2, lines 10-20, and the first cache miss is in the first process. The reference of Hendel as stated above teaches of FIFO being a form of resource.

Per claim 30, and 50, the detail of prefetch instruction from memory is described in Okin in col. 3, lines 45-61.

Per claims 24, 69 and 70, Okin teaches of re-execution of the suspended process in col. claim 7 (switching back to execute the first process when the memory is available).

Per claims 31 and 51, in the system of Okin decode instruction is before the execution instruction and it is shown in Fig. 1A (see blocks 3-4, and 5-6).

Per claims 34-36, and 54-56, Okin disclose a system for switching the context of state elements of a very fast processor within a clock cycle. The processor disclosed does not know what kind of instruction it is processing, therefore, it is obvious to use Okin's processor for any environment including network data for the reason to minimize the average instruction cycle time for the processor with a main memory access time exceeding processor clock cycle. The system of Hendel discloses a networking environment wherein the command and status interface unit further comprises **command routing means** for selectively **routing the receive commands to the first FIFO storage unit, the transmit commands to the second FIFO storage unit, miscellaneous commands** to the medium access control unit, and clearing commands to the third and fourth FIFO storage units. Later he teaches of request FIFO, command FIFO, and status FIFO in col. 10, lines 55, line 55 to col. 11, line 7. Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to use Okin's modified

processor in the networking environment of Hendel, for the reason to minimize the average instruction cycle time for the processor with a main memory access time.

4. Claims 19-22, 25-29, 37-45, 57-64, 66-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okin (U.S.Pat, No. 5,361,337, Okin) in view of Hendel et al. (U.S.Pat, No. 5,175,732, Hendel), and further in view of Nemirovsky (DYNAMIC INSTRUCTION STREAM COMPUTER, Apple Computer Corporation, 1991, Dr. Mario Daniel Nemirovsky).

Per claims 37 and 57, the processor of Claim 17 wherein when the first instruction is aborted, the processor is operable to suspend the first task and to execute another task instead of the first task while the first task is suspended. The system of Okin fails to explicitly teach of the limitation, However, Nemirovsky, teaches of dynamic interleaving in a pipeline processing environment wherein a task can be executed when a first task is suspended (See page 166, under dynamic interleaving, even when interrupts are invoked, other task can be running). Therefore, it would have been obvious for a person ordinary skill in the art at the time the invention was made to use Nemirovsky's interleaving method in Okin's processor because it will eliminate the overhead of context switching and by doing that efficiency will be increased.

Per claim 38, and 58, the processor of Claim 37 wherein suspension of the first task and scheduling of the other task instead of the first task does not involve instruction execution by the processor. The method of Nemirovsky does not require instruction execution.

Per claim 39, and 59, the processor of Claim 37 wherein the first task remains suspended at least until the resource becomes available to the first task. The system of Okin teaches of the limitation in claim 4, lines 19-26 (the processor within one clock cycle to finish the first process if the necessary data had been retrieved from the main memory).

Per claim 25, the system of Okin teaches multitasking in col. 2, lines 10-20, and the first cache miss is in the first process. The reference of Hendel as stated above teaches of FIFO being a form of resource.

Per claims 19, see the rejection of claim 14 above.

Per claims 20 and 27, see Okin, col. 3, lines 28-44, and the rejection of claim 39 above.

Per claims 21, 26, and 28, see Okin, col. 3, lines 45-61.

Per claims 22 and 29, see Okin, col. 4, lines 1-26.

Per claim 40, the system of Okin teaches of interleaving of the tasks in a pipeline-processing environment (see, Nemirovsky, page 165, R. col. section 3.4). In there tasks from different group can be interleaved. Therefore, when the first instruction from the first task is suspended, another task from another group is executed.

Per claims 41 and 60, see the pipeline interleaving section in Nemirovsky (See page 166, under dynamic interleaving, even when interrupts are invoked, other task can be running).

Per claims 42 and 61, the environment of Okin is a pipeline processing environment (see col. 3, lines 28-44, and the suspension of the instruction in a task in a pipeline is shown in claims 1, and 2.

Per claims 43 and 62, in the system of Okin decode instruction is before the execution instruction and it is shown in Fig. 1A (see blocks 3-4, and 5-6).

Per claims 44 and 63, see Okin, a multiplexer 29 is coupled to a plurality of write-read buffer 30--30". The plurality of write-read buffer are in turn coupled to a plurality of register files 32--32" over a multiplexer 31. Before data flows from the plurality of register files 32--32" to the ALSU 36, they are channeled over multiplexers 33, 33", and 34.

Per claims 45 and 64, interleaving is a way to share processor resources between multiple processes (see Nemirovsky, page 165, left col. Section 3.3).

Per claims 66-68, please see the rejection of claims 34-36 section 4 above.

5. Claims 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hough (U.S.Pat. No. 4,604,649, 'Hough'), in view of Tanenbaum (Structured Computer Organization).

A multi-tasking processor comprising task scheduling circuitry, such that when a task TAI executed by the processor starts to execute a first instruction accessing a resource

which is unavailable to the task TAI due to the resource being made available to another task, the task scheduling circuitry suspends execution of the first instruction after starting to execute the first instruction and suspends the task TA1 at least until the resource becomes available to the task TA1 (see Hough, abs., and col. 3, lines 5-9, and col. 3 67 to col. 4, line 11), and if another task TA2 is ready for execution in place of the task TA1 when the resource is unavailable to the task TA1, the task scheduling circuitry schedules the task TA2. The system of Hough fails to explicitly teach of "wherein the task scheduling circuitry operation does not involve instruction execution by the processor". However, as Tanenbaum suggest (See pages 11-12), many computer operations including task synchronization could be implemented in microprogram where they were originally were explicitly programmed at the conventional machine level. Therefore, it would have been obvious to implement the scheduling technique of Hough in microporgram as well as hardware, for the reason to save registers and make the system more efficient.

6. Claims 46-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hough (U.S.Pat. No. 4,604,649, 'Hough'), in view of in view of Tanenbaum (Structured Computer Organization), further in view of Hendel et al. (U.S.Pat, No. 5,175,732, Hendel).

Per claims 46-49, the system of Hough fails to explicitly teach of FIFO as a resource, however, the system of Hendel discloses a networking environment wherein the command and status interface unit further comprises **command routing means** for selectively **routing the receive commands to the first FIFO storage unit, the transmit commands to the second FIFO storage unit, miscellaneous commands** to the medium

access control unit, and clearing commands to the third and fourth FIFO storage units. Later he teaches of request FIFO, command FIFO, and status FIFO in col. 10, lines 55, line 55 to col. 11, line 7. Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to use Hough processor in the networking environment of Hendel, for the reason to minimize the average instruction cycle time for the processor with a main memory access time.

7. Applicant on page 10 of his Remarks arguing that:

> "The four cited references do not teach or suggest a FIFO accessing instruction that
> can be blocked after the processor has started its execution as recited in Claim 14. Hendel's processor 4 writes commands to FIFOs 25, 26 (Fig. 5 and column 10, lines 10-15 and 30-35). Hendel's MAC 17 reads and executes these commands and writes status bits to FIFOs 27, 28. Hendel, column 10, lines 50-51 and 55-61. The status bits are always available to the processor and can be inspected by the processor "at any time" (column 13, line 55; column 14, line 10). Thus, the processor can determine at any time if the earlier receive or transmit command has been executed and the corresponding FIFO is available. The processor can make this determination before accessing the FIFO, and Hendel does not teach or suggest a FIFO accessing instruction, which can be blocked after the processor, started its execution if the FIF'O is unavailable as recited in Claim 14.
> Okin, Uchiyama and Nemirovsky also do not teach or suggest an instruction as in claim 14."

In response, this argument is not persuasive because, the reference of Okin teaches of cache miss, which is a condition where the process has access to the resource (a form of resource). Therefore, it is executing while it encounter the unavailability of a resource. Additionally, the reference of Hendel is not relied for the suspension of a process (or a task) upon unavailability of a resource (or another resource such as a FIFO). The

rejection is based on two references and not one. Regarding the argument of "instruction in claim 14", it must be pointed out that creating a hardware that perform the functionality of a software does not constitute a patentable invention. In other words it is the designers decision to implement some of the features in hardware based on any reason that make his system more efficient. The Examiner is citing the reference of "Tanenbaum", to show many features that could be implemented as hardware instructions (See Tanenbaum, page 11 last paragraph to page 12, one paragraph to the last).

Applicant on page 11 arguing that:

> "Claim 18 recites a task TAI executing an instruction accessing a resource that may be unavailable to the task TAI due to the resource being made available to another task. The instruction execution can start even if the resource is unavailable to the task TAI, when the resource is unavailable due to it being made available to the other task. The instruction execution is suspended after its execution has been started, and the task TAI is suspended. Some embodiments of Claim 18 facilitate task synchronization needed to access a shared resource because a task can execute an instruction accessing the resource without first determining if the resource is unavailable due to its being made available to another task. Claim 18 is not limited to the embodiments or advantages discussed herein.
> Okin's cache misses are unrelated to the cache being made available to another process or task as recited in Claim 18. Okin therefore does not teach or suggest the instruction of Claim 18".

In response, applicant's attention is respectfully directed to the rejection of claim 18 in this office action and rejection of claim 18 in view of Hough. The reference of Hough teaches of "task synchronization accessing a shared resource without first determining if the resource is unavailable due to its being made available to another task" in col. 3, line 67 to col. 4, line 11, task must be suspended or resumed for the lack of availability or the reappearance of availability of a resource).

Regarding the synchronization being implemented without the use of semaphore, it is submitted that there is not such limitation in the claims. Applicant is arguing a feature of the invention not specifically stated in the claim language, which is improper.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure

8.Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Majid A. Banankhah** whose telephone number is (571) **272-3770**. The examiner can normally be reached on Monday – Thursday, 8:00 AM – 4:00 PM.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756.
Information regarding the status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Maid Banankhah

2/16/05

MAJID BANANKHAH
PRIMARY EXAMINER